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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,222	09/02/2004	Edward W. Conrad	BUR920030067US1	5221

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EXAMINER	
MOFFAT, JONATHAN	
ART UNIT	**PAPER NUMBER**
2863	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,222	CONRAD ET AL.	
	Examiner	Art Unit	
	Jonathan Moffat	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/2/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/2/2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/2/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 3 and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). In addition, there is an unlabeled item in Fig 1, which appears to be a sensor or inspection apparatus. Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. These objections to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8-10, 12-14, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Templeton (US pat 6,269,322).

With respect to claim 1, Templeton discloses a method comprising:

1) Providing a plurality of artifacts on the wafer stage outside of the area where a substrate can be placed on the wafer stage, the artifacts are placed a known distance apart from each other (Figs 11a-d).

2) Measuring the distance between the artifacts with the alignment system (column 7 1st paragraph and Fig 11f).

3) Comparing the measured distance to the known distance to calibrate the grid parameters of the wafer stage (column 4 lines 45-60).

With respect to claim 2, Templeton discloses the measuring step includes:

1) Moving a first of the artifacts to the alignment system (Fig 9 and column 3 lines 6-10).

2) Using the alignment system to measure the location of the first of the artifacts (Fig 11f and column 3 lines 10-15).

3) Moving a second of the artifacts to the alignment system (Fig 9 and column 3 lines 6-10).

4) Using the alignment system to measure the location of the second of the artifacts (Fig 11f and column 3 lines 10-15).

With respect to claim 3, Templeton discloses the measuring step includes the further step of using said measurements of the location of the first and second of the artifacts to determine the measured distance between the first and second of the artifacts (Fig 11f).

With respect to claim 4, Templeton discloses the providing step includes the steps of:

1) Locating a first of the artifacts on a first side of said area (Figs 11a-b).

2) Locating a second of the artifacts on a second side of said area, said second side being opposite said first side (Figs 11a-b).

With respect to claim 5, Templeton discloses both of said first and second artifacts are located on a common axis (Figs 11a-b).

With respect to claim 8, Templeton discloses a method comprising:

1) Positioning a wafer on the stage ().

2) Providing a plurality of artifacts on the wafer stage outside the wafer, the artifacts being a known distance apart from each other (Figs 11a-b and column 8 line 20).

3) Positioning a first of the artifacts at a determined location relative to the alignment system (Fig 9 item 160 and column 3 lines 6-10).

4) Moving the wafer stage a predetermined distance and forming a first structure on the wafer (Figs 12 and 13).

5) Positioning a second of the artifacts at a defined location relative to the alignment system (Fig 9 item 160 and column 3 lines 6-10).

6) Moving the wafer stage a predetermined distance and forming a second structure on the wafer (Figs 12 and 13).

7) Measuring the offset between said first and second structures to calibrate the grid parameters of the wafer stage (Fig 14).

With respect to claim 9, Templeton discloses the step of providing the plurality of artifacts includes the step of positioning the first and second of the artifacts on a common axis, on opposite sides of the wafer (Figs 11a and 11b).

With respect to claim 10, Templeton discloses the step of forming the second structure includes the step of forming the second structure on top of the first structure (Figs 12 and 13).

With respect to claim 11, Templeton discloses the first and second structures are spaced apart and the steps of:

1) Forming another pair of structures on the wafer (column 4 lines 60-67 and fig 13).

2) Measuring the distance between said another pair of structures and using the measured distance between said another pair of structures to determine the difference between field and grid parameters (column 3 lines 21-38).

3) Using the measured offset between the first and second structures to provide the grid parameters (Fig 14).

With respect to claim 12, Templeton discloses an apparatus comprising:

1) A plurality of artifacts on the wafer stage outside of the area where a substrate can be placed on the wafer stage, the artifacts are placed a known distance apart from each other (Figs 11a-b, and column 8 line 20).

2) Means for measuring the distance between the artifacts (Fig 9 item 200).

3) Means for comparing the measured distance to the calibrate the grid parameters of the wafer stage (column 3 lines 21-38).

With respect to claim 13, Templeton discloses the photolithography tool further includes an alignment system, and the measuring means includes:

1) Means for moving a first and a second of the artifacts to the alignment system (Fig 9 item 160).

2) Means for using the alignment system to measure the locations of the of the artifacts (column 4 lines 35-45).

3) Means for using said measurements of the locations of the first and second of the artifacts to determine the measured distance between the first and second of the artifacts (column 2 lines 50-55).

With respect to claim 14, Templeton discloses the apparatus wherein the first and second of the artifacts are located on a common axis on opposite sides of said area (Figs 11a and 11b).

With respect to claim 16, Templeton discloses an apparatus comprising:

1) A plurality of artifacts on the wafer stage outside of the wafer, the artifacts being a known distance apart from each other (Figs 11a and11b).

2) Means for positioning a first and a second of the artifacts at defined locations relative to the alignment system, and for moving the wafer stage predetermined distances from said defined locations (Fig 9 item 160 and column 3 lines 6-10).

3) Means for forming first and second structures on the wafer, after said wafer stage has been moved said predetermined distances (Figs 12 and 13 and column 2 lines 50-53).

4) Means for measuring the offset between said first and second structures to calibrate the grid parameters of the wafer stage (column 2 lines 50-60).

With respect to claim 17, Templeton discloses the first and second of the artifacts are on a common axis, on opposite sides of the wafer (Figs 11a and 11b).

With respect to claim 18, Templeton discloses an apparatus wherein:

1) Said first and second structures are spaced apart (column 4 lines 1-3).

2) Said means for forming are used to form another pair of structures on the wafer (Figs 12 and 13 and column 2 lines 50-53).

3) Said measuring means are used to measure the distance between said another pair of structures to use the measured distance between said another pair of structures to determine the difference between field and grid parameters, and to use the measured offset between the first and second structures to provide the grid parameters (Fig 14 and column 3 lines 21-38).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-7, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Templeton as applied to claims 1 and 12 above, in view of Chu (US pat 5,734,594).

With respect to claim 6, Templeton discloses a method comprising providing a first pair of artifacts a known distance apart from each other (Figs 11a-11b). Templeton further discloses measuring the distance between the first pair of artifacts (column 2 lines 50-55).

Templeton fails to disclose providing and measuring a second pair of artifacts.

Chu teaches providing a second pair of artifacts a known distance apart from each other (Fig 1a). Chu further teaches measuring the distance between the second pair of artifacts (Fig 5).

It would have been obvious to one of ordinary skill in the art to combine the method of Chu into the method of Templeton by adding a second set of calibration marks and repeating the same steps a second time for this second pair of marks. This would increase the accuracy of the calibration.

With respect to claim 7, Templeton discloses the step of providing the first pair of artifacts includes the step of locating said first pair of artifacts on a first axis on opposite sides of said area (Figs 11a and 11b).

Templeton fails to disclose a second pair of artifacts.

Chu teaches the step of providing the second pair of artifacts includes the step of locating said second pair of artifacts on a second axis, on opposite sides of said area and said second axis is perpendicular to the first axis (Fig 1a).

It would have been obvious to one of ordinary skill in the art to combine the method of Chu into the method of Templeton by adding a second set of calibration marks and repeating the same steps a second time for this second pair of marks. This would increase the accuracy of the calibration. Further it would have been obvious to locate the second set of marks on a perpendicular axis in order to calibrate the wafer in two dimensions.

With respect to claim 15, Templeton discloses a first pair of artifacts a known distance apart from each other on a first axis and on opposite sides of said area (Figs 11a and 11b and column 8 line 20).

Templeton fails to disclose a second pair of artifacts and measuring the distance between both pairs.

Chu teaches a second pair of artifacts a known distance apart from each other on a second axis and on opposite sides of said area (Fig 1a), and the measuring means includes means for measuring the distance between the first pair of artifacts and the distance between the second pair of artifacts (Fig 5).

It would have been obvious to one of ordinary skill in the art to combine the method of Chu into the method of Templeton by adding a second set of calibration marks and repeating the same steps a second time for this second pair of marks. This would increase the accuracy of the calibration.

Conclusion

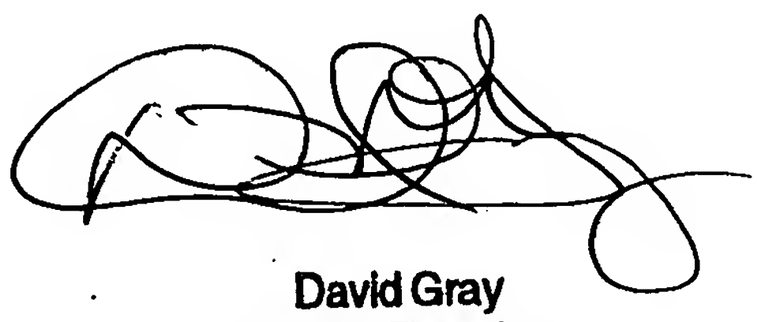
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dietmayer (US pat 6,418,388) and Leroux (US pat pub 20040138842).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan Moffat whose telephone number is (571) 272-2255. The examiner can normally be reached on Mon-Fri, from 7:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JM



David Gray
Primary Examiner